Institute of Engineering & Management

Dept. of Information Technology

B.Tech (5th Semester) Assignment 2018

Computer Architecture (IT-502)

Answer all the questions:

1. Prepare a report of case study on "Taxonomy of parallel computers" taking specific cases of at least 5 parallel computers. (15)

2. Explain the significance of MMX. Differentiate a data flow computer from a control flow computer with suitable area of application. (5+5)

3. Design the space-time diagram of a Superscalar processor of degree '3'. Find out the speedup factor of a Superscalar processor of degree 'n' using 'k' stage pipeline. (5)

4. a) Differentiate simple cycles and greedy cycles. If the dynamic pipeline clock rate is 20 MHz and the value of MAL is 2 then find out the throughput. What is MIPS? (10)

   b) A non- pipeline system takes 40ns to process a task. The same task can be processed in a 4 segment pipeline with a clock cycle of 10ns Determine the speed up ratio of the pipeline for 50 tasks. What is the maximum speedup that can be achieved in this case? (5)

5. Analyze the performance of VLIW architecture over Superscalar processor. (5)

6. What is the significance of a Vector Processor? Design the space time diagram of a vector processor. (5)

7. Consider the following reservation table:

	1	2	3	4
S1	X			X
S2		X		
S3			X	

   Write down the forbidden latencies and initial collision vector. Draw the state diagram for scheduling the Pipeline. Find out the simple and greedy cycle and MAL. If the pipeline clock rate is 25 MHz then what is the throughput of the Pipeline. What are the bounds on MAL. (3+3+3+3+3)

8. a) A virtual memory system has the following specifications:
   - Size of the virtual address space is 64 KB
   - Size of the physical address space is 4 KB
   - Page size is 512-byte

From the following page table, what are the physical addresses corresponding to the virtual addresses:

i) 3494 ii) 12350 iii) 30123

Page number	Frame No
0	0
3	1
7	2
4	3
10	4
12	5
24	6
30	7

b) Consider a computer system with a 32- bit logical address and 4KB page size. The system supports up to 512 MB of physical memory. How many entries are there in a conventional single-level page table? (5+5)

9. a) Assume a main memory size of 32K x 12, cache memory of size 512 x 12 and block size of 1 word. For direct mapping what would be the size of the tag and index field?

   b) Compare the advantages and disadvantages of direct mapping and associative mapping. (5+5)

10. a) Describe two switch settings of and 8x8 omega Network without blocking build with 2x2 switches with following permutations:

    $\pi = (0,7,6,4,2)\ (1,3)(5)$

    b) A system with 4-word set associative cache has 128 blocks in the cache memory, each block contains 16 words (8 bit words) and the main memory has 16384 words. How many blocks are there in the main memory and what is the size of tag field? (5+5)